REMARKS

Claims 1-9 are pending in the case. Claims 1-8 are rejected. Claim 9 is objected to as being dependent upon a rejected base claim but is allowable if rewritten in independent form. In the present submission, Applicant has amended the specification to update references to related applications. Reconsideration is respectfully requested.

Specification

The Examiner objected to the specification because application numbers for referenced patent applications were not included. In the present submission, the specification has been amended and all application serial numbers have been updated.

§103(a) Rejection

Claims 1-8 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Ogata et al. (U.S. Patent No. 6,753,910; hereafter "Ogata"). The Examiner contends that Ogata discloses some of the limitations of the claims while official notice was taken of claim elements not shown in Ogata. Applicant respectfully traverses the rejection.

Ogata is directed to an image processing apparatus and an image processing method where the gradation of the image data is corrected while effectively preventing a finally obtained image from partial deterioration of the contrast. (See Abstract of Ogata.) Ogata shows in Figure 1 a television camera which is described as follows:

> The television camera is generally denoted at 1 and includes **a CCD solid-state image pickup device 2**…the television camera 1 further includes **a memory 4N** which…temporarily holds and stores the image pickup result VN by normal exposure.
>
> The television camera 1 further includes **a memory 4S** which…temporarily holds and stores the image pickup result VS by shorter time exposure…**A level correction circuit 6** corrects a pixel value…so that the image pickup result VT from the addition circuit 5 may have a linearity sufficient for practical use, and outputs the corrected pixel value…A **gradation correction circuit 8** corrects the pixel value of the image pickup result VT to correct the gradation of the image pickup result VT and outputs the image pickup result VT of the corrected gradation. **A signal processing**

> **circuit 9** following the gradation correction circuit 8 executes various signal processes necessary for the television camera to obtain an image pickup result and outputs the image pickup result to an external apparatus. (Ogata, col. 4, ln. 22, to col. 5, ln. 23; emphasis added.)

Ogata describes a complete television camera system where image data is obtained by a CCD device and stored in memories 4N/4S. Memories 4N and 4S are operationally equivalent and they are merely used to store image data of different exposure times. Then the image data is level corrected and gradation corrected before being provided to a signal processing circuit 9. In Ogata's image processing system, only memories 4N/4S are used to temporarily hold and store the image data from the CCD device. Processing of the image data by level correction circuit 6, gradation correction circuit 8 and signal processing circuit 9 must therefore be derived from the data stored in memories 4N/4S. Ogata does not use a separate frame buffer for image processing.

Claim 1

Claim 1, as amended, recites:

> 1. A digital imaging system, comprising:
> **an image sensor comprising a two-dimensional array of pixel elements and an image buffer** for storing pixel data of each captured image, said image sensor outputting digital signals on a pixel bus as pixel data representing an image of a scene;
> **an interface circuit** coupled to receive said pixel data from said pixel bus;
> **a frame buffer**, in communication with said interface circuit, coupled to store pixel data provided by said interface circuit; and
> **an image processor for processing said pixel data stored in said frame buffer** to generate image data for displaying said image of said scene,
> wherein said interface circuit comprises a noise reduction circuit performing signal processing on said pixel data received on said pixel bus for noise reduction. (Emphasis added.)

Claim 1 is patentable over Ogata at least by reciting "an image sensor comprising a two-dimensional array of pixel elements and an image buffer," "a frame buffer, in communication with said interface circuit," and "an image processor for processing said pixel data stored in said frame buffer." Claim 1 recites a digital imaging system including an image sensor and an

image processor and a digital interface for communication between the image sensor and the image processor. The architecture of the digital imaging system of claim 1 is shown in Figure 1 of Applicant's specification. The imaging system architecture of in claim 1 uses an image buffer to store pixel data for each captured image and a frame buffer to store pixel data for image processing. The advantages of using two memories in the digital imaging system of claim 1 are explained in Applicant's specification as follows:

> In one embodiment, the video imaging system of the present invention is formed as two integrated circuits. That is, the video imaging system includes a digital image sensor chip and a digital image processor chip. **A fully digital communication interface** is provided to permit high speed and high fidelity data transfer between the digital image sensor and the digital signal processor…The video imaging system includes **two memory circuits for storing the image data**. Specifically, **an image buffer is included in the digital image sensor for storing the image data of each captured image and a frame buffer in the digital image processor for storing the image data from the image sensor for processing**. **Because a second memory circuit is included**, the video imaging system of the present invention can perform temporal filtering of the image data using the second memory circuit (the frame buffer) to improve image quality. (Applicant's specification, paragraph [0037]; emphasis added.)

As presently amended to clarify the claim, claim 1 now recites using an image buffer to store the capture image data and a frame buffer for storing pixel data for processing. The interface circuit is situated between these two memories and performs noise reduction operations.

Ogata does not teach or suggest using two memories to support the storage and processing of the image data. If memories 4N/4S are taken as the image buffer of claim 1, then the CCD stores image data in the image buffer while signal processing circuit 9 also operate on the pixel data in the image buffer. This system configuration is patentably distinct from that recited in claim 1. If memories 4N/4S are taken as the frame buffer of claim 1, then the gradation correction circuit 8 of Ogata cannot meet the element of the interface circuit of claim 1 as the interface circuit must be between the CCD and the frame buffer.

Furthermore, the Examiner agrees that Ogata does not expressly teach the limitations of a frame buffer and an image processor as recited in claim 1. The Examiner then proceeded to take Official Notice that "it is well known at the time the invention was made to process

pixel data for display purposes." From this Official Notice, the Examiner contends that it should be obvious to include a frame buffer and an image processor in the same manner as recited in claim 1. (See Office Action, p. 3.)

Applicant hereby respectfully traverses the Examiner's assertion of official notice. ***Applicant submits that the factual assertion by the Examiner is not properly officially noticed and not properly based upon common knowledge***. In accordance with MPEP §2144.03, Applicant demands the Examiner to provide documentary evidence supporting the Official Notice in the next Office Action if the rejection is to be maintained. The error in the Examiner's action is as follows.

MPEP §2144.03 states that: "It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known." While official notice may be taken of a fact that is asserted to be "common knowledge" without specific reliance on documentary evidence, such official notice may be taken only where the fact noticed was readily verifiable or **where there was nothing of record to contradict it**. (See MPEP §2144.03.)

Even if we assume *arguendo* that the Examiner's Official Notice is appropriate to the extent that it is well known to process pixel data for display, the Official Notice does not and cannot extend to cover the specific system architecture used by each skilled artisan to perform such image processing. Each skilled artisan may come up with different systems and methods for performing the image processing. The case in point is the Ogata reference, the art of record. Ogata describes one way of implementing an image processing apparatus where only one memory (4N or 4S) is used to store pixel data from the CCD and where the data stored in the single memory is also used by the gradation correction circuit and the signal processing circuit for image processing.

The teaching in Ogata is in direct contradiction to the claimed invention of claim 1. Claim 1 recites a system where an image buffer is used to store data from the image sensor and a frame buffer is used to store data from the interface circuit and where ***the image processor operates on the data stored in the frame buffer***. While the Examiner may take Official Notice of the fact that it is well known to perform image processing, the Examiner may not take Official Notice of the specific ways that a skilled artisan would implement such image processing. Therefore, unless the Examiner can provide documentary evidence to

support his Official Notice, the Examiner's assertion of official notice with regard to claim 1 is improper and must be withdrawn.

For the above reasons, claim 1 is patentable over Ogata, alone or in combination with the Official Notice taken by the Examiner.

Claims 2-8

Claims 2-8, dependent upon claim 1, are patentable over Ogata for at least the same reasons claim 1 is patentable.

Claim 9

Claim 9 is objected to as being dependent upon a rejected base claim but is allowable if rewritten in independent form. For the above reasons, because claim 1 is patentable, claim 9 is therefore also in condition for allowance.

CONCLUSION

In the present submission, claim 1 has been amended. The amendments to the specification made herein deal only with clerical matters. No new matter has been entered. Accordingly, claims 1-9 are in condition for allowance. If the Examiner would like to discuss any aspect of this application, the Examiner is invited to contact the undersigned at (408) 382-0480.

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/Carmen C Cook/	January 12, 2007
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Respectfully submitted,

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